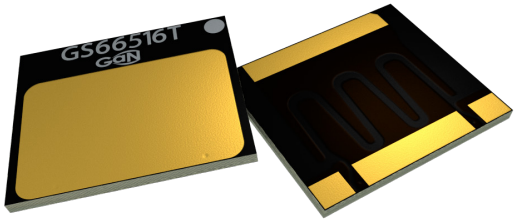
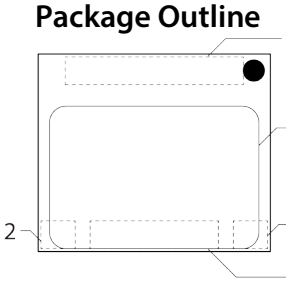
Features

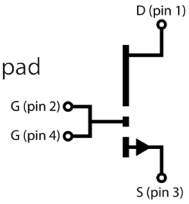
- 650 V enhancement mode power switch
- Top-side cooled configuration
- $R_{DS(on)}$ = 25 mΩ
- $I_{DS(max)}$ = 60 A
- Ultra-low FOM Island Technology™ die
- Low inductance GaN*PX*™ package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 9 x 7.6 mm^2 PCB footprint
- Dual gate pads for optimal board layout
- RoHS 6 compliant



Package Outline



Circuit Symbol



The thermal pad is internally connected to Source (S- pin 3) and substrate

Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- 400 V input DC-DC converters
- On Board Battery Chargers
- Traction Drive

Description

The GS66516T is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*™** packaging enables low inductance & low thermal resistance in a small package. The GS66516T is a top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain-to-Source Voltage (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	60	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	47	A

(1) For 1 µs, duty cycle D<0.1

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$		0.3		°C /W
Thermal Resistance (junction-to-board)	$R_{\Theta JB}$		3.0		°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}			260	°C

Ordering Information

Part number	Package type	Ordering code	Packing method	Quantity
GS66516T	GaN*PX*™ Top-Side Cooled	GS66516T-TR	Tape-and-reel	2500
GS66516T	GaN*PX*™ Top-Side Cooled	GS66516T-MR	Mini-reel	250

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 100 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	mΩ	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 18 A
Drain-to-Source On Resistance	$R_{DS(on)}$		65		mΩ	V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_D = 14 mA
Gate-to-Source Current	I_{GS}		320		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.0		V	V_{DS} = 400 V, I_D = 60 A
Drain-to-Source Leakage Current	I_{DSS}		4	100	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		800		µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 150 °C
Internal Gate Resistance	R_G		1.5		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		520		pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{OSS}		130		pF	
Reverse Transfer Capacitance	C_{RSS}		4		pF	
Effective Output Capacitance, Energy Related (Note 3)	$C_{O(ER)}$		177		pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (Note 4)	$C_{O(TR)}$		284		pF	
Total Gate Charge	Q_G		12.1		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		4.4		nC	
Gate-to-Drain Charge	Q_{GD}		3.4		nC	
Output Charge	Q_{OSS}		113		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics continued (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.6		ns	V_{DD} = 400 V, V_{GS} = 0 - 6 V, I_D = 16 A, $R_{G(ext)}$ = 5 Ω, T_J = 25 °C (note 5)
Rise Time	t_R		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	t_F		22		ns	
Output Capacitance Stored Energy	E_{OSS}		14.1		µJ	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz
Switching Energy during turn-on	E_{on}		134.1		µJ	V_{DS} = 400 V, I_{DS} = 20 A, V_{GS} = 0-6 V, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 1 Ω, L = 120 µH, L_P = 10 nH (notes 6, 7)
Switching Energy during turn-off	E_{off}		14.7		µJ	

(5) See Figure 12 for timing test circuit diagram and definition waveforms
(6) L_P = parasitic inductance
(7) See Figure 13 for switching test circuit

Electrical Performance Graphs

GS66516T I_{DS} vs. V_{DS} Characteristic

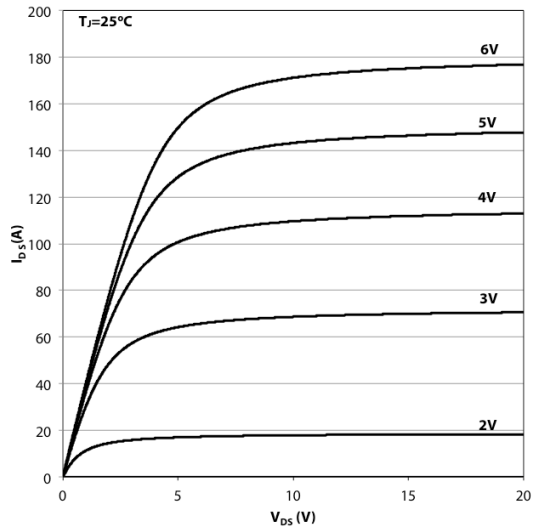


Figure 1 : Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

GS66516T I_{DS} vs. V_{DS} Characteristic

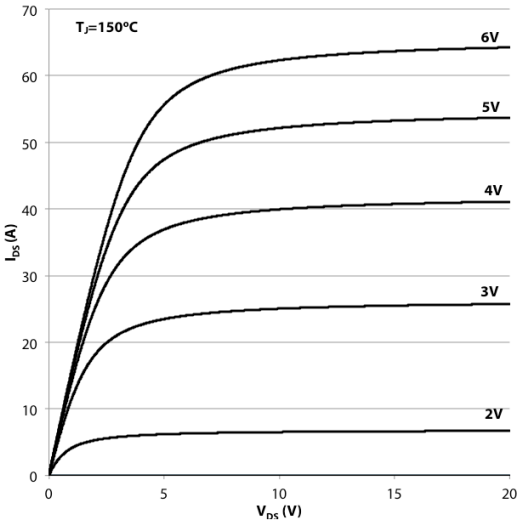


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

$R_{DS(on)}$ vs. I_{DS} Characteristic

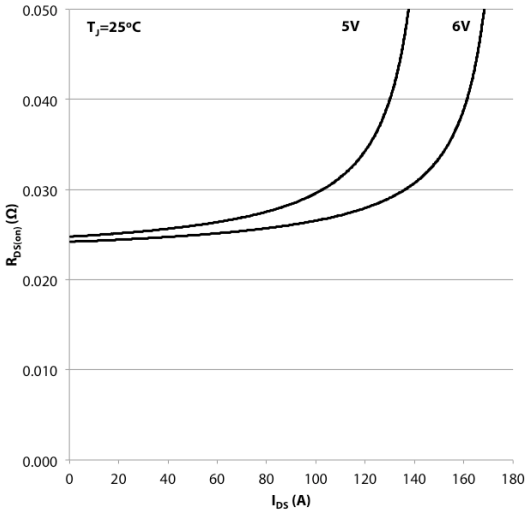


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

$R_{DS(on)}$ vs. I_{DS} Characteristic

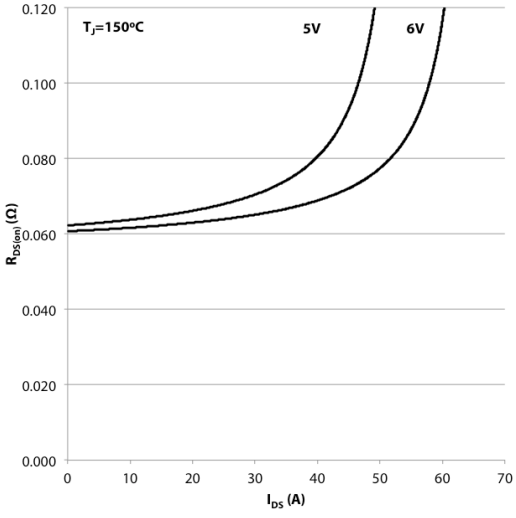


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150°C

Electrical Performance Graphs

GS66516T I_{DS} vs. V_{DS} , T_J dependence

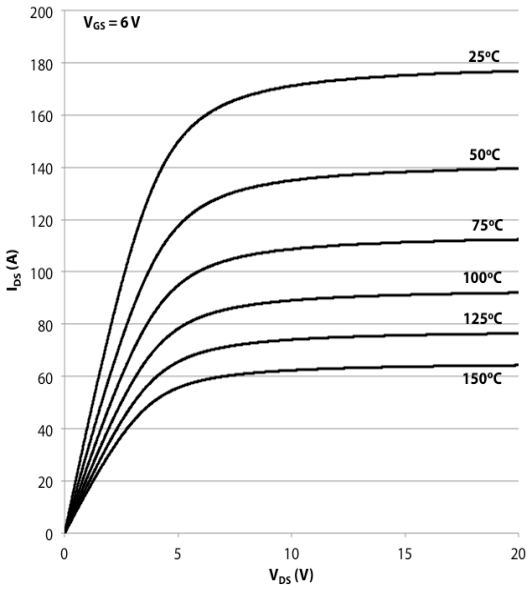


Figure 5 : Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

GS66516T Gate Charge, Q_G Characteristic

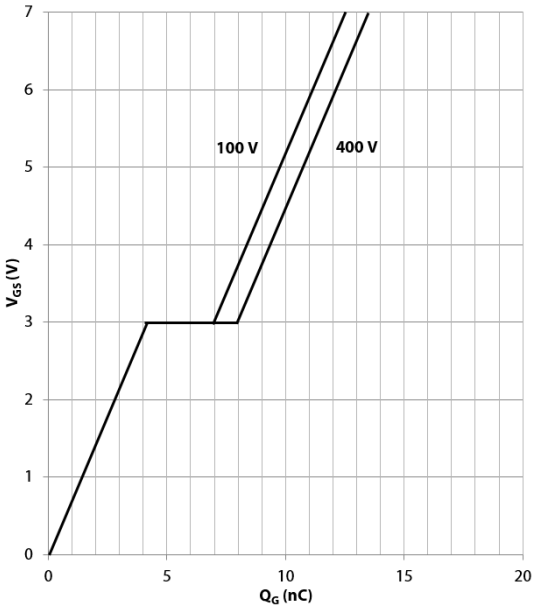


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 100, 400 V

GS66516T Capacitance Characteristics

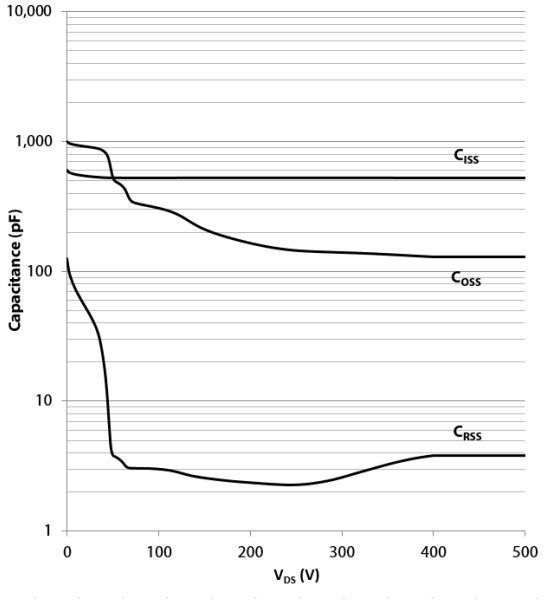


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS66516T Stored Energy Characteristic

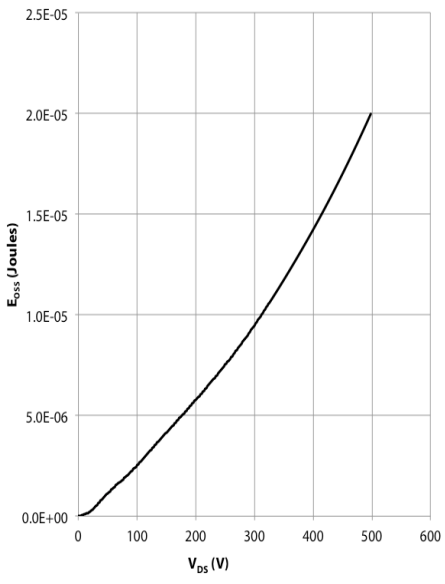


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

GS66516T Reverse Conduction Characteristics

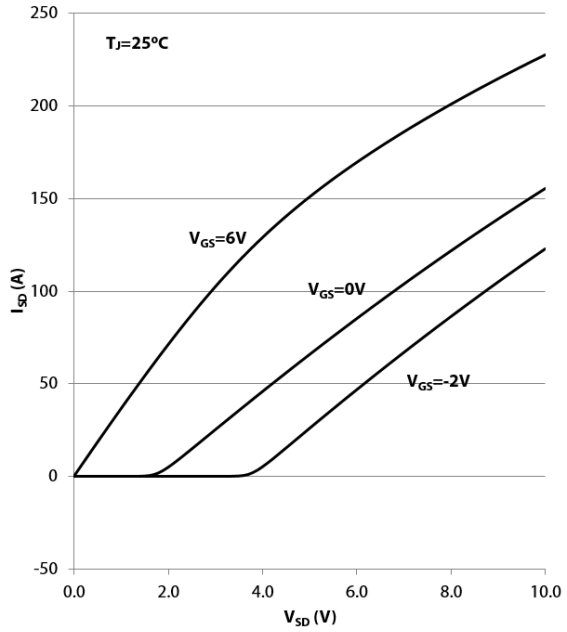


Figure 9 : Typical I_{SD} vs. V_{SD}

GS66516T I_{DS} vs. V_{GS} Characteristic

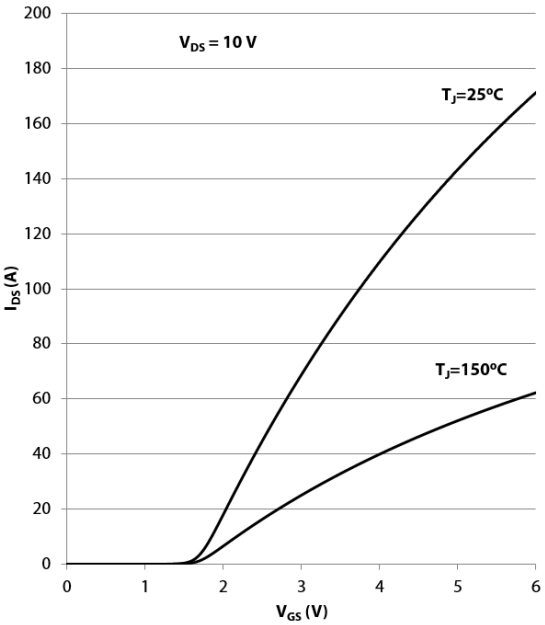


Figure 10 : Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

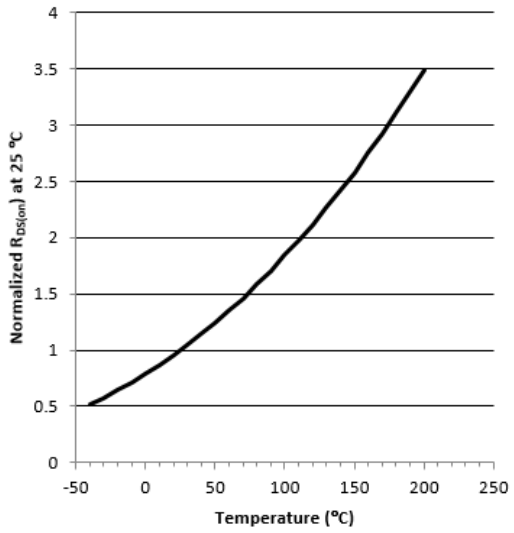


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

Test Circuits

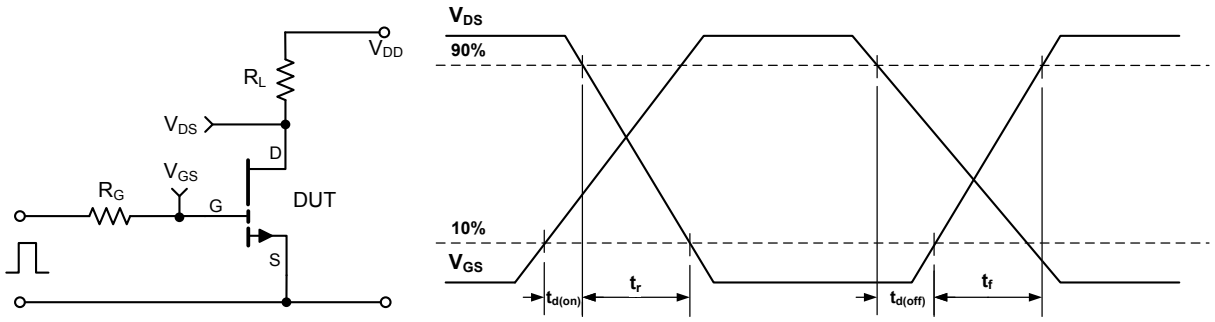


Figure 12: GS66516T switching time test circuit and waveforms

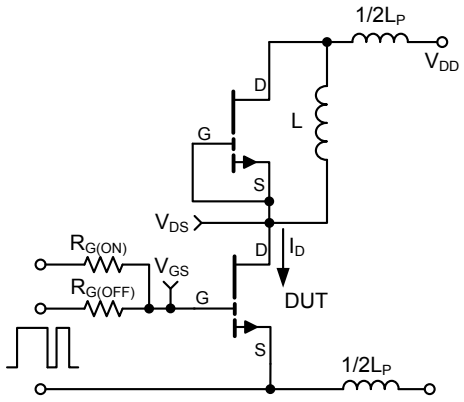


Figure 13: GS66516T Switching Loss Test Circuit

Thermal Performance Graphs

GS66516T I_{DS} - V_{DS} SOA

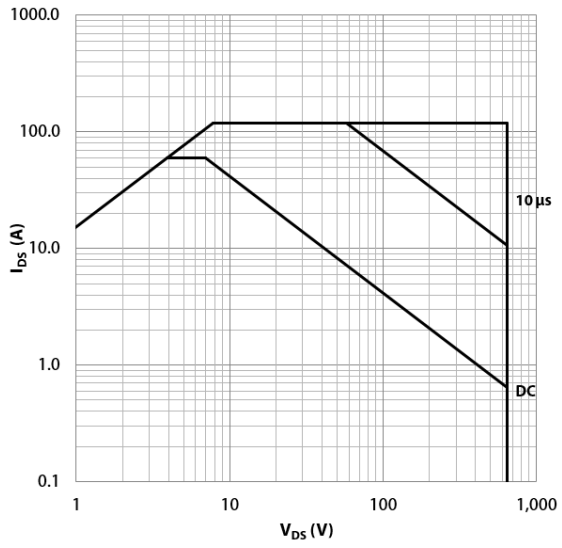


Figure 14: Safe Operating Area @ T_{case} = 25 °C

GS66516T Power Dissipation – Temperature Derating

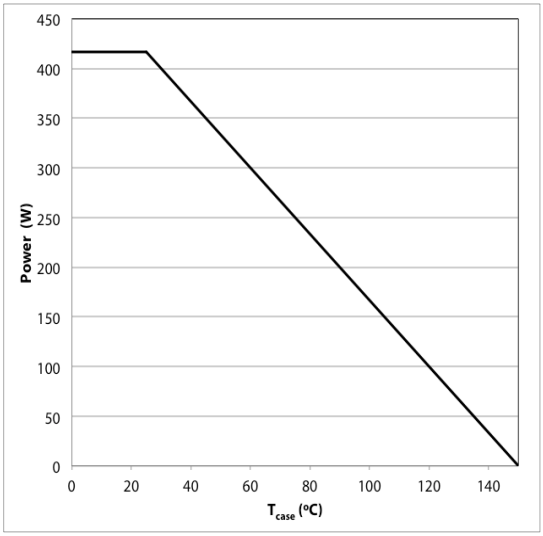


Figure 15: Derating vs. Case Temperature

GS66516T Transient $R_{\theta JC}$

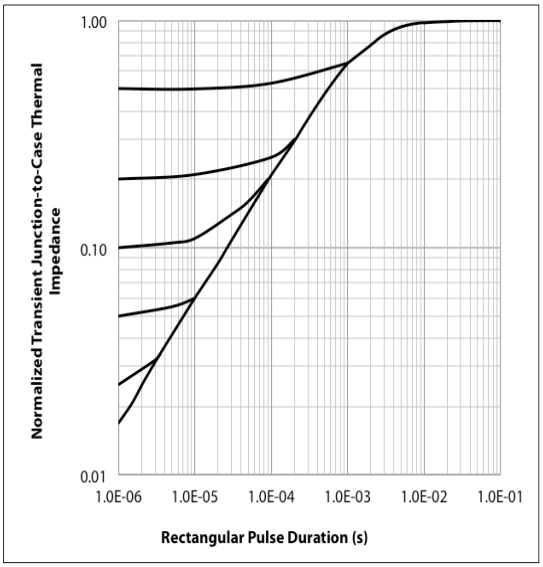


Figure 16: Transient Thermal Impedance

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs and duty cycle, D, < 0.1. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note GN001 for more details.

Parallel Operation

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the GS66516T top-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible. GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

Although the GS66516T does not have a dedicated source sense pin, the GaN*PX*™ packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection on the PCB to the Source pad in a kelvin configuration, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

Thermal

The substrate is internally connected to the thermal pad on the top-side and to the source pin on the bottom side of the GS66516T. The transistor is designed to be cooled using a heat sink on the top of the device.
The Drain and Source pads are not as thermally conductive as a thermal pad. However adding more copper under these two pads will improve thermal performance by reducing the packaging temperature.

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (V_{GD}) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750V for 1 µs with a duty cycle D < 0.1 is acceptable.

Packaging and Soldering

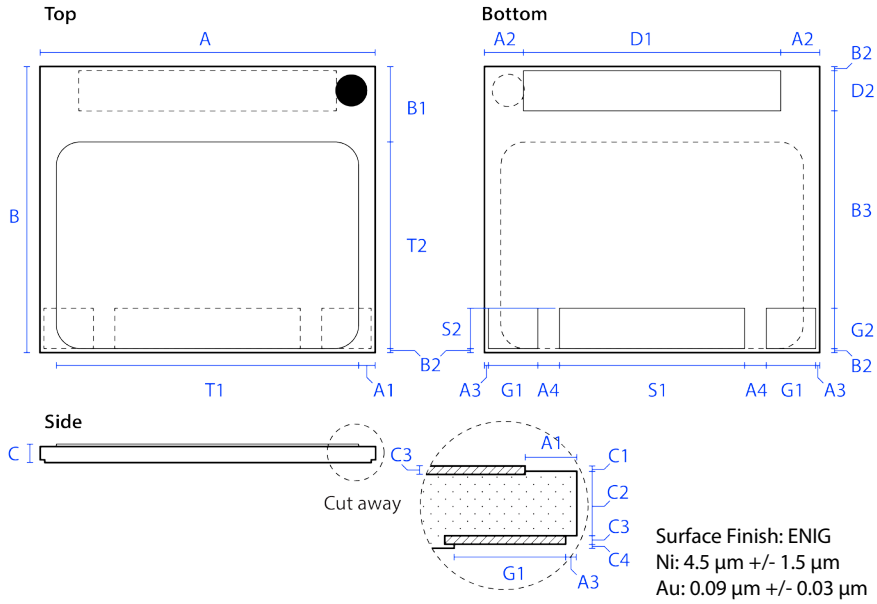
The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66516T device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

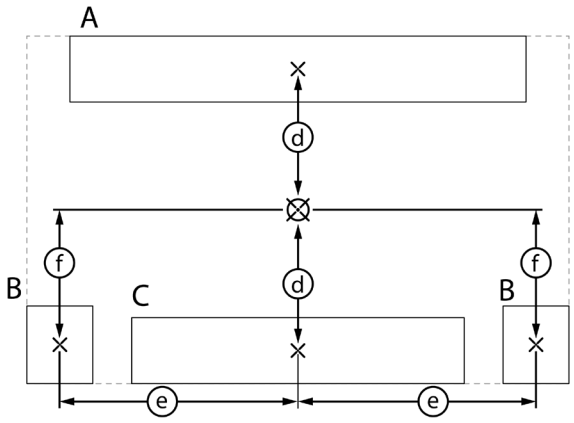
Package Dimensions



	mm	Inches	
A	9.00	0.354	± 0.10 mm (0.004″)
A1	0.365	0.014	± 0.05 mm (0.002″)
A2	1.03	0.041	± 0.05 mm (0.002″)
A3	0.075	0.003	± 0.05 mm (0.002″)
A4	0.59	0.023	
B	7.64	0.301	± 0.10 mm (0.004″)
B1	1.925	0.076	± 0.05 mm (0.002″)
B2	0.075	0.003	± 0.05 mm (0.002″)
B3	5.39	0.212	
C	0.54	0.0213	± 0.05 mm (0.002″)
C1	0.04	0.0016	
C2	0.40	0.0157	
C3	0.07	0.0028	
C4	0.03	0.0012	
D1	6.94	0.273	
D2	1.05	0.041	
G1	1.30	0.051	
G2	1.05	0.041	
S1	5.07	0.200	
S2	1.05	0.041	
T1	8.27	0.033	
T2	5.64	0.222	

Note: Inch measurements are approximate values

Recommended Minimum Footprint for Printed Circuit Board



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	5.81	0.84	0.229	0.033
B	0.84	0.99	0.033	0.039
C	4.24	0.84	0.167	0.033

Dimensions

	mm	Inches
d	1.80	0.071
e	3.04	0.120
f	1.72	0.068

PCB pad openings

Package outline